CENTRO DE ENSEÑANZA TÉCNICA Y SUPERIOR

Colegio de Ingeniería
Dirección de Posgrado
Campus Mexicali

Proyecto de Ingeniería e Innovación

“A Proposed Design of a Process Method to Eliminate RF test Fixture Mismatch Issues is presented”

para obtener el grado de

Maestría en Ingeniería e Innovación

Presenta

Enrico Marcelo Sy

Director de proyecto: Dra. Dania Licea Verduzco

Co-director de proyecto: Dr. Luis C. Básaca Preciado

Asesor Industria: Zelman Hernandez Castro, MBA

Mexicali, Baja California. Junio del 2018

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Comité evaluador:

MC. Cristóbal Capiz Gómez	Dr. Miguel A. Salinas Yáñez	Dr. Miguel A. Ponce Camacho

Mexicali, Baja California. Junio del 2018

DEDICATION

This work is dedicated in loving memory of my mom who encouraged and supported me through thick and thin providing me guidance, wisdom and patience when needed.

As I continue on my path, she will always be remembered with a grateful heart.

To my loving wife Virginia and to my thoughtful and kind daughter Daniele Rose
You are a gift to me from God Almighty

ACKNOWLEDGEMENTS

This research would not have been possible without the support and guidance of our Instructor Professor Dra. Dania Licea Verduzco, Coordinador de Ingeniería en Diseño Gráfico Digital Escuela de Ingeniería, campus Mexicali. Skyworks Solutions manager and directors: JH Whang, Luis Solis and Zelman Hernandez who approved, coordinated and worked hard to make this study in Masters in Engineering and Innovation a success. For the financial support Skyworks has extended to us, for this i will always be grateful. The government of Mexico for the financial support extended as well thru CONACYT scholarship program.

Above all else, I am thankful to our God Almighty, the source of wisdom, knowledge and understanding.

Abstract

RF final test measurements include the DC to RF performance of components and are therefore included on the system offsets measurements to compensate for the deviations. The equivalent RF circuit of a test fixture involves parasitics and is complex; it can be lumped as a series or parallel circuit model, which represents the real and imaginary resistive and reactive parts of total equivalent circuit impedance. These parasitic components that greatly affect RF performance are significantly influenced by an uncontrolled variable such as the environmental factor. An environmental factor affects the behavior of the Radio Frequencies and microwave signals and impacts the parametric measured values. These measured value inconsistencies can result in incorrectly passing or failing products during the final test, such as when performing design validation, characterization and qualification before transitioning to final test production process. During test production set-up, often times a fixture-tester mismatch is encountered as an effect on measurement error as an added parasitic catalyst when humidity is introduced.

This proposed project goal is to eliminate tester mismatch problem that are encountered on the test floor. This project is also completed in fulfillment for the requirement in Master's Degree program in Engineering and Innovation. To achieve this, a new process method is proposed to provide solution to the existing problem that the current method does not consider. This proposed method is based on the experiment that was done thru simulations and circuit modeling where the test fixture is injected with a known level of power of different frequencies at the test points and measurements are taken on the adjacent pins. These procedures mimic the effects of the parasitic components on the RF signal performance within the fixture when it is installed on the automatic test equipment.

Keywords:

Measured value, environmental factor, Radio Frequency (RF), parametric, scattering parameters, fixture board, automatic test equipment (ATE), printed circuit board (PCB), parasitic components. RF performance,

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Postgraduate Management
Mexicali Campus

INFORMS:

That the master's thesis entitled, "A **Proposed Design of a Process Method to Eliminate RF test Fixture Mismatch Issues is presented** ", under the direction and supervision of Cetys Academic Assessor Dania Licea Verduzco, has been successfully carried out by :

Eng. Enrico Sy Marcelo
Matricula: **M033009**

The project is accepted and considered relevant achieving significant results in the Test Department. Furthermore, the project is aligned to Skyworks Solutions de Mexico's mission, vision, and objectives. Managerial support for the application of the project has been provided with the commitment of the employee to fulfill the objective mentioned in the details of the project.

Sincerely

_____

MBA. Zelman Hernandez Castro
TEST ENGINEERING DIRECTOR

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1 Introduction

Semiconductor manufacturing facilities ensures the quality and reliability of the products being delivered to customers by subjecting every Integrated Circuit (IC) to a rigorous application test methodologies. The final test is the last procedure the devices under test (DUT) has to pass through and are segregated as PASS, FAIL and several other bins for different types of categories. This final test setup contains 3 basic hardware components, the automatic test equipment (ATE), fixture board, and the device under test (DUT) which is the integrated circuit (IC) device product.

As shown on the Figure 1, the test fixture board is a printed circuit board (PCB) with socket and components that make the device under test (DUT) operate to its specified function during the testing process. The test fixture board functions as an interface that interconnects the end product device or Device under test (DUT) and the Automatic Test Equipment (ATE).

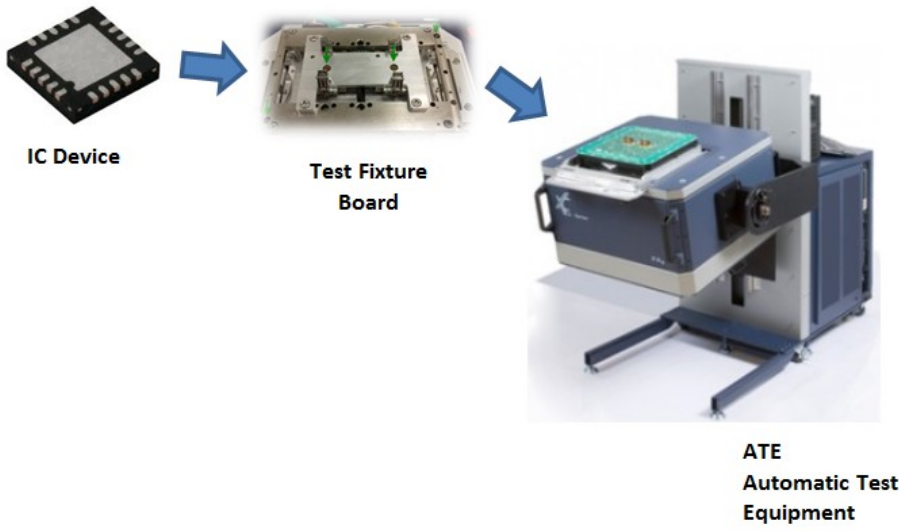


Figure 1 Basic Final Test Configuration

Source: own illustration*; Tester image* (LTXC, 2018).

During qualification, characterization, and correlation activities, the device under test (DUT) is placed on the socket that is installed on the test fixture board. Moreover, while the test fixture is mounted on the tester ATE, the test program is being executed for

functional and parametric characterization and measurement. These characterization activities are done on all test fixtures on the several testers. After the test fixtures have been qualified, these are then stored in a storage area and will only be used until the device lot fabrication has been completed for mass production.

The problem in encountered by the engineers and technicians whenever several production tasks are being set up for manufacturing process. During the setup activities which include undertakings such as correlation of golden unit, some test fixture boards that previously had passed characterization and correlation processes exhibits a failure that inhibits the fixture to be used on the ATE systems. This is the issue that is called the fixture – tester mismatch. The fixture – tester mismatch is then defined as the test fixture that used to pass on the ATE systems either no longer passes on the same system or on other ATE systems though the characterization and correlation activities were previously performed thoroughly.

The result of study and experiments conducted on this project study expound the factors that have adverse effects on the RF performance. And this RF performance drains down to the most basic circuit analysis which is the circuit impedance. Impedance is a vital parameter in characterizing RF circuits, components, and the materials that are utilized to build components.

1.0.1 Present fixture cleaning and staging procedure

To describe the present method of cleaning after the fixture boards are repaired and or modification were done; the fixture boards are cleansed with alcohol and wiped with an industrial cleaner wipes. The fixtures are then dried up with a compressed dry air (CDA) and often times are left to dry up alone by itself. This method may seems to be an legitimate means of cleaning the fixture boards after repair but this method leaves the surface and VIAS of the circuit with a residues from fluxes. And consequently, the dried flux residues are capable of adsorbing the moist in a humid environment. The adsorbent capability of the flux stores the moist on the surface of the traces and on the

components offering an added value to the impurities of the parasitics of the components and transmission line.

In a strictly controlled environment such as the test manufacturing 100K cleanroom facilities, humidity may circulate not coming from the ventilation of the building but thru the air that peoples breathe, heat exhausting from human bodies and other potential sources. The fixtures are then stored in a container and then placed on the hardware stock room for safekeeping.

As illustrated on Figures 2, 3 and 4, the surface of the board reveals the presence of humidity or moist on the surface of the board. It can be seen that the board has a residue of the flux and it has adsorbed moist on the air. As shown on Figure 4, this moist on flux residue not only can be observed thru the sense of sight but also thru the sense of touch. Tragically, the circuit impedance changes as the parasitics of the components is altered. In effect, and the circuit may no longer in an impedance of 50 Ohms as it is originally designed. This effect may not be realized in a DC and low frequency measurement but is significant on higher RF and especially on the microwave spectrum. The effects of the humidity on the fixture boards are random as measurement varies depending on the variables which are the amount of moist present, the area of the coverage on the components that were involved on the measurements. The frequency of measurement may affect only certain frequency ranges and the power level when the measurement was verified.

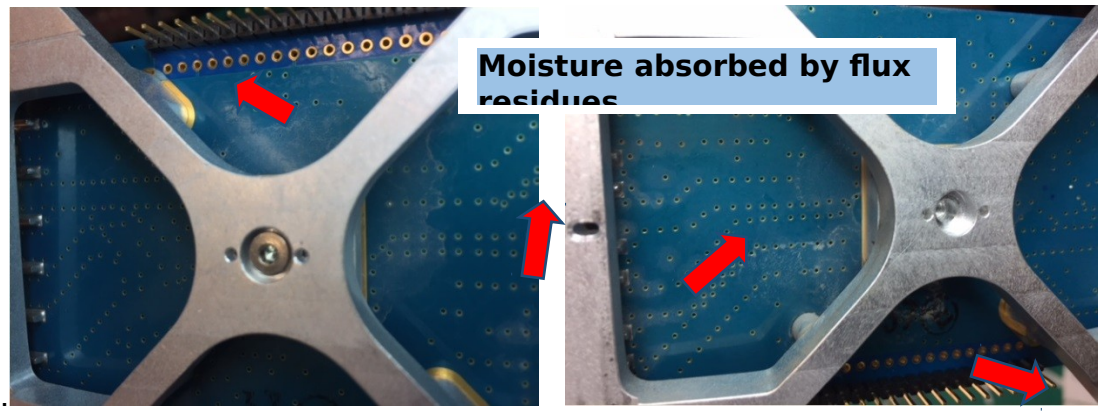


Figure 2 Rear views of the fixture board 1 showing flux residues with adsorbed humidity

Source: own illustration

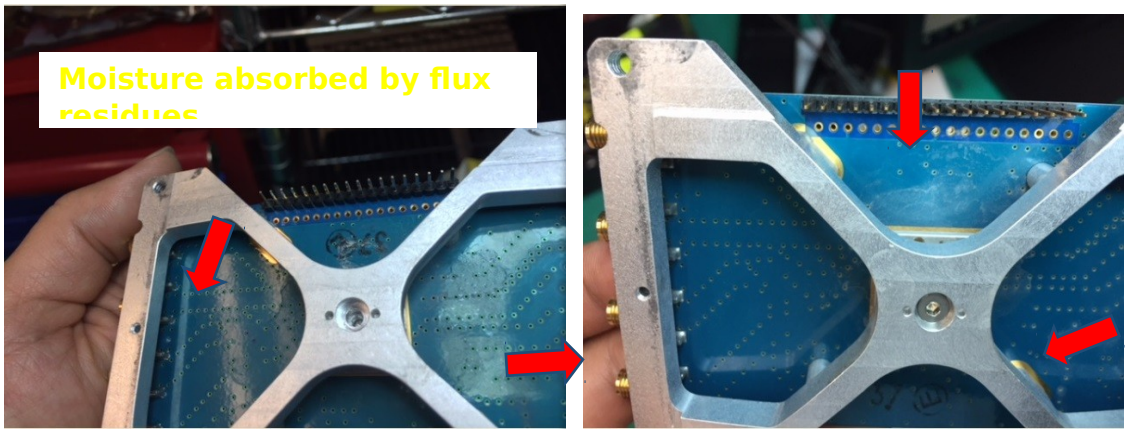


Figure 3 Rear views of the fixture board 2 showing flux residues with adsorbed humidity

Source: own illustration

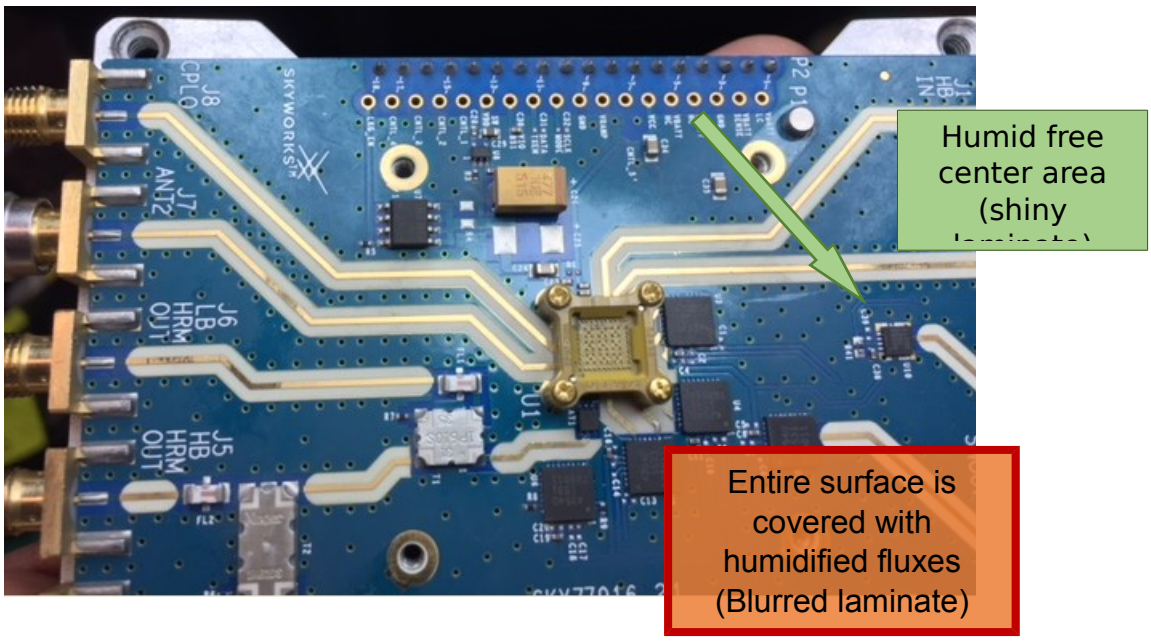


Figure 4 Components Capacitor, Inductor, Resistor and control Integrated Circuits are covered with humid fluxes

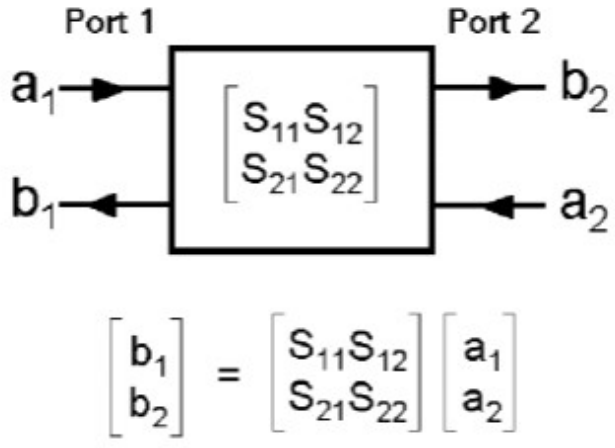
Source: own illustration

The result of these environmental effects are numerous and unpredictable. The fixture may intermittently fail during set up as the measured value has deviated from the acquired data during verification and qualification. A fixture RF performance is influenced by parasitic components by some degree on every components exhibits potential unpredictable results.

The S-parameters of a network provide a clear physical interpretation of the transmission and reflection performance of the device. The S-parameters for a two-port network are defined using the reflected or emanating waves, b1 and b2, as the dependent variables, and the incident waves, a1 and a2, as the independent variables (Agilent Technologies, 2001, 2004). (Figure 5) The general equations for these waves as a function of the S-parameters are shown below on equation 1.

$$b1 = S11a1 + S12a2 \qquad \text{Eq. 1}$$
$$b2 = S21a1 + S22a2$$

Using these equations, the individual S-parameters can be determined by taking the ratio of the reflected or transmitted wave to the incident wave with a perfect termination placed at the output as demonstrated on Figure 5. (Agilent Technologies, 2001, 2004).



$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} S_{12} \\ S_{21} S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

Figure 5 Representation of a two –Port S- parameter network

Source: (Agilent Technologies, 2001, 2004)

1.1 Background

Equipment uptime and efficiency issues in a manufacturing company must be seriously taken into account since they can cause a loss in company revenue with serious consequences affecting the integrity on the delivery of committed products to customer. In particular, when we are dealing with industrial tool which is the Over-all Equipment Efficiency (OEE) measurement, apart from the regular process and reduced yield issues, the recurring availability loss that is attributed caused by the set-up time is considered. The set up time loss may be categorized into different classifications such as shown on Figure 6.

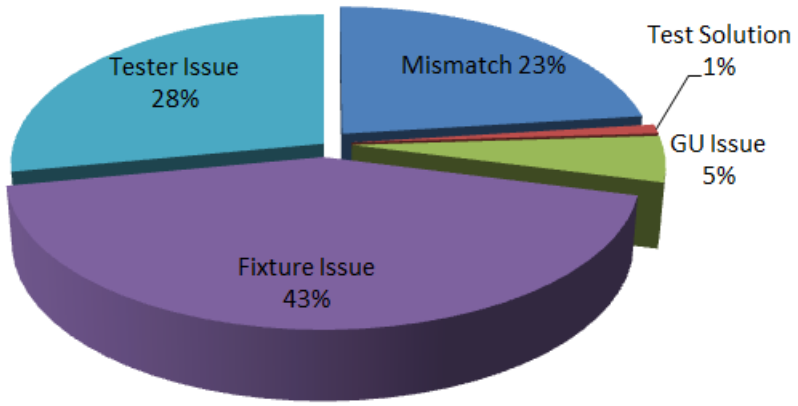


Figure 6 Set up Downtime Summary from June to August 2017

Source: Own illustration; data from Skyworks Engineering Data

1.1.1 Emphasis of the study

The focus of this project is the elimination of the mismatch issue that which contributes to almost one fourth of the total set up downtime, one of the main factors that affects over all Equipment Efficiency (OEE). Consequently, tackling this issue poses an increase in set up time efficiency.

In order to lessen the availability loss of the automatic test equipment (ATE) caused by the increased in set-up time from a known failure contributor - the Fixture-to-Tester

mismatch, a study was conducted on the fixtures that has an intermittent mismatch failure. The RF parameters were taken into account as this kind of issue is known to surface only with the RF performance. The root cause is determined thru analysis of the data collected from a simulated and repeatable experiment. The variables affecting the correlated fixture to fail where considered on this experiment as the effect of such are equally significant when used on an Automatic Test Equipment (ATE). The root cause must be determined, isolated and therefore be given a solution that would eliminate the recurrence of such availability loss.

1.2 Justification

The study about the RF test fixture failing on the testers after it was qualified for production use is essential and timely. The fact that technology advances rapidly with complexity, the more it is going to be difficult to manage the failures related to Fixture-Tester correlation in the future. As the method of measurement involved in the test process are enhanced continuously, the set up Engineers and technicians may encounter often of this same kind of issues during RF devices Test production set up. Nevertheless, if the variables and root cause of the failure are identified and isolated, this kind of issue is expected to be eliminated if not minimized to an acceptable level. The knowledge in tackling this problem will equip the engineers and technicians to resolve this kind of issues rapidly whenever this is encountered. Thereby the intricacy of evolving set up techniques of RF devices for production readiness will no longer be contributing to the availability loss. To identify the variables causing the fixture-tester correlation failure could mean a gateway to a controlled and manageable fixture – tester match issues.

1.3 Statement of Problem

On October 1, 2017, the first quarter of this fiscal year 2018, Final Test production department is faced with an uptrend on the test equipment availability loss, the significant periods of time in which equipment is scheduled for running in production but is not due to the increase on set-up time. Production maintenance Engineers and technicians are encountering a Fixture-to-tester mismatch issue where the supposed qualified fixture to one of the Automatic Test Equipment (ATE) is expected to run on another same type of ATE but is encountering failures on several RF test parameters.

There are several unanswered questions regarding the set-up failure relating to the fixture to tester mismatch. And top management disagrees over the long set up time and without a tangible resolution to the issue. This is because the increase in equipment availability loss could mean a higher product output loss that translates to the company financial loss as a consequence. It is a fact that if this fixture to tester correlation are left without a permanent control and is not managed correctly may start a chain reaction and affect other set up relation issues. The stir caused by uncontrolled variables suggests that Engineers have not explored all sides of the availability loss concerning fixture-tester correlation.

1.4 Research Question

Based on the problem described on this paper, the following research question is established:

What are the factors and variables induced in the present method that may have caused the fixture to fail during production setup and what new method can be implemented to eliminate the fixture-tester mismatch problem?

1.4.1 Sub questions

1. What are the external factors that could have been introduced on the test fixture for it to perform differently on different ATE equipment specifically on RF test parameters?

2. What new method or process that needs to be designed to prevent the occurrence of the fixture-tester problem?

1.5 General Objective

Basing from the research question, the general objective is defined:

To design a method or process flow that would ensure the prevention of the occurrence of the fixture-tester mismatch problem when utilized on similar ATE systems. In order to derive a method or process, the root cause will have to be isolated and its characteristic is analyzed.

1.5.1 Specific Objective

1. Identify the external factors that are causing the fixture-tester mismatch problem to exist during the production setups.

2. Develop a new method, process or controls that will to eliminate the existence of the fixture-tester mismatch during production setups.

1.6 Hypothesis

1. An environmental factor such as the humidity affects RF performance of the fixture as the “real value” of the components and transmission lines intrinsically fluctuates with the additional residual effects of the humidity on its surface.

2. The presence of the solder fluxes on the surface of the fixture and on the components magnifies the existence and effect of humidity due to its adsorptive property.

2 Theoretical Frameworks

The real value takes into consideration the effects of a component's parasitics (Figure 9). The real value represents effective impedance, which a real-world component exhibits. The real value is the algebraic sum of the circuit component's resistive and reactive vectors, which come from the principal element (deemed as a pure element)

and the parasitics. Since the parasitics yield a different impedance vector for a different frequency, the real value is frequency dependent (Keysight Technologies, 2016). Consequently, taking RF measurements on the fixture board that was not exposed to humidity may deliver a different RF measurement data compared to that of the fixture board that is exposed to environmental factor such as humidity.

Since the beginning of RF and millimeter wave (uW) development and its Test applications, engineers, designers and developers have long been struggling with RF performance's random behavior. In relation to the RF performance mentioned, the problem defined on this paper can well describe this unpredictable behavior on the Test production environment as; a fixture to tester mismatch issue. It is a dilemma where the RF fixture board that has passed vigorous testing during validation and qualification, this same fixture unexpectedly encounters an off set on these parametric RF measurements after the board has momentarily stored or un utilized before production testing resumes. This has been a common predicament in an RF design and test industries even up to this time. There has been no direct and conclusive studies conducted previously and thereby this research study focuses on this issue and provides a process method to eliminate such. Digging on into the root cause of the fixture to tester mismatch offers and in depth understanding on how the issue surfaces and in effect aids to prevent such predicament in the future.

Several research studies that was carried out previously and that this research is referenced to, studies that investigate and analyze the effect of humidity on the RF and microwave frequencies. The information garnered from these research studies support the theory of this paper. One of these research is the propagation of the RF signals on the transmission lines authored by Richard Fawley and Patricia Ferrie of Teledyne Defense Ltd, Shipley, England, "The effects of moisture on the performance of a highly sensitive microwave transmission line frequency discriminator" (Fawley & Ferrie, 2012) in which they describe their work that is carried out to investigate the relationship between the variation in the transmission line physical characteristics

particularly the changes in the effective electrical of the delay line medium caused by moisture.

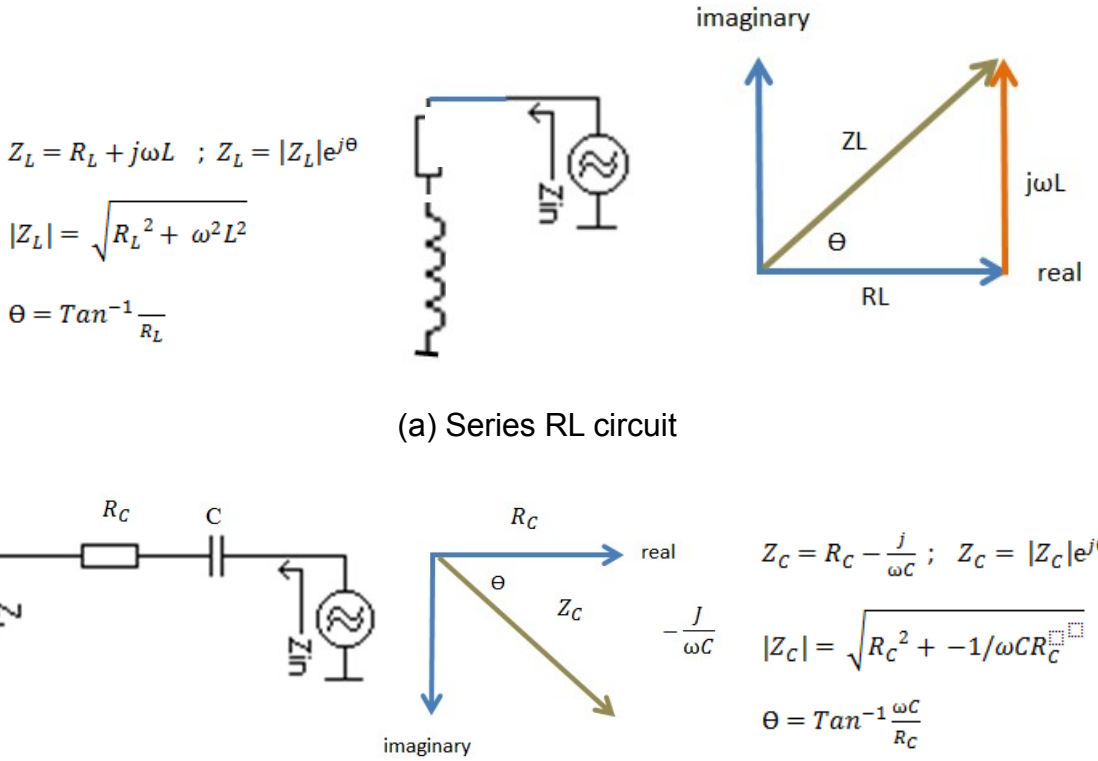
Another previous research papers conducted relating to this study such as an experiment and investigation performed. “Effect of Humidity on Dielectric Charging Process in Electrostatic Capacitive RF MEMS Switches Based on Kelvin Probe Force Microscopy Surface Potential Measurements” (Zaghloul, Papaioannou, Coccetti, Pons, & Plana, 2009), which is similar to the study being conducted but is completely different from the way the experiment is performed as the previous research focused their investigation on the effect of the relative humidity on the dielectric charging process in PECVD silicon nitride and is based on the surface potential measurements from Kelvin Probe Force Microscopy. And their investigation reveals that the potential distribution was found to be more confined as the relative humidity decreases especially at smaller charge injection bias. While this paper focuses on the study of the effect of humidity on the test fixture by measuring the power transferred from GND pin to the input and output pins on the printed circuit board (PCB) using the Spectrum and Network Analyzers.

Other studies were also considered and referred to as their theories is relevant to this research which is also associated with the effect on humidity. K. Fukunaga and S. Kurahashi and their research paper “Dielectric Properties of Printed Circuit Board Insulations at Microwaves and Millimeter Waves” (Fukunaga & Kurahashi, 2007, pp. 1-3). They measured the complex permittivity of various polymeric materials used as the insulation layers of PCBs from 1 MHz to 110 GHz using various measurement systems. Their experimental results also proved that the permittivity is strongly influenced by humidity. Their paper is focused on the dielectric and is different from the study being conducted which focuses on the effect of humidity on the test fixtures RF measurements.

Keysight Technology handbook, also discusses the effect of humidity on the calibration of the Test instruments. Keysight impedance measurement handbook describes humidity effects to have a much greater influence on measurement accuracy at high frequency than in low frequency impedance measurements stating that instrument accuracy is determined by “the degree to which the observed performance of an instrument is affected by humidity” (Keysight Technologies, 2016).

Other previous research papers on which this study are referred to, evaluat es and performed their experiments on the effect of environmental factor using different experiment procedures but having similar goals as this research study were conducted, “ TEMPERATURE AND HUMIDITY DRIFT CHARACTERIZATION OF PASSIVE RF COMPONENTS FOR A TWO-TONE CALIBRATION METHOD” (Janas, Czuba, Mavric, & Schlarb, 2016). They performed drift characterization of a set of RF components, which could serve for implementation of a signal injection circuit and their study concluded that synchronization to a low noise electrical source is corrupted by a phase detection error originating in the electrical components and connections due to thermal and humidity-related drifts. Similarly, these observed effects were observed on this study though the procedure of the experiments conducted in dissimilar.

As a continuation, Impedance (Z), in general, is defined as the total opposition or acceptance a circuit or components creates to the flow of an alternating current (AC) for a specific frequency. As illustrated on Figure 7, It is represented as a complex form of quantity that is graphically displayed on a vector plane (Pozar, 1998).



(a) Series RL circuit

(b) Series RC circuit

Figure 7 Impedance (Z) consists of real part (R) and imaginary part (jω)

Source: own illustration *and theory by* (Pozar, 1998)

An impedance vector consists of a real part (R, resistance) and an imaginary part (jω, reactance) as shown in Figure 6. Impedance can be expressed using the rectangular-coordinate form R + jω or in the polar form as a magnitude and phase angle: |Z|_ θ.

Figure 8 also shows the mathematical relationship between R, X, |Z|, and θ. In some cases, using the reciprocal of impedance is mathematically expedient. In which case 1/Z = 1/(R + jX) = Y = G + jB, where Y represents admittance, G conductance, and B Susceptance. The unit of impedance is the ohm (Ω), and admittance is the Siemen (S). Impedance is a commonly used parameter and is especially useful for representing a series connection of resistance and reactance, because it can be expressed simply as a sum, R and X. For a parallel connection, it is better to use admittance (see Figure 8) (Keysight Technologies, 2016).

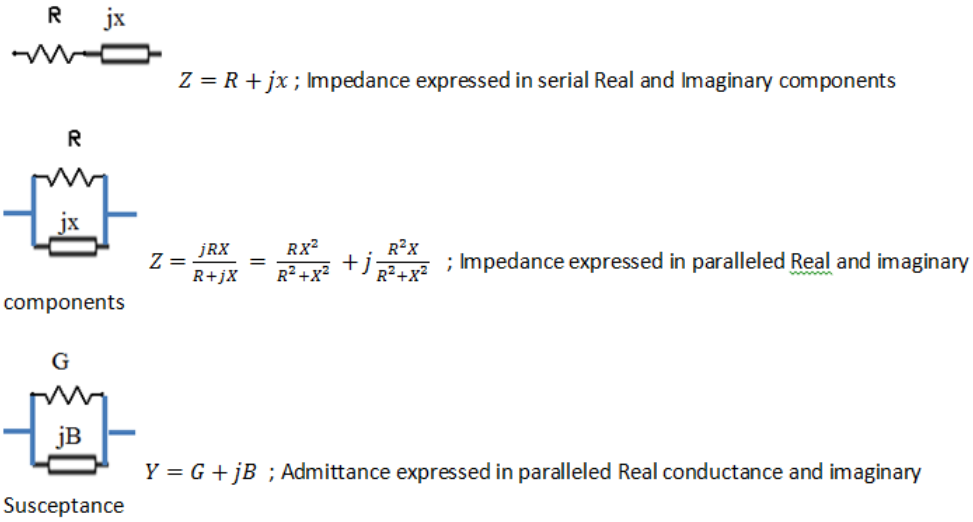


Figure 8 Expression of series and parallel combination of real and imaginary components

Source: own illustration

In a real world, all circuit components are neither purely resistive, nor purely reactive. They involve both of these impedance elements and all real-world devices have parasitics—unwanted inductance in resistors, unwanted resistance in capacitors, unwanted capacitance in inductors, etc. Most parasitics reside in components, affecting both a component's usefulness and the accuracy with which you can determine its resistance, capacitance, or inductance. With the combination of the component's primary element and parasitics, a component will be like a complex circuit, if it is represented by an equivalent circuit model as shown in Figure 9 (Balanis C. A., 2016).

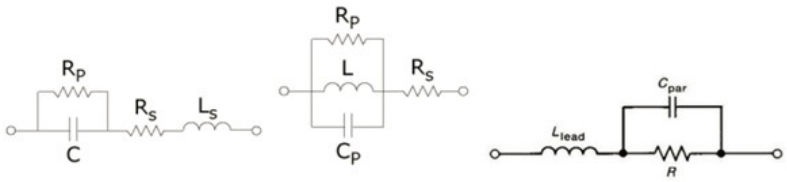


Figure 9 Components Capacitor, Inductor ad Resistor with parasitic represented by an electrical equivalent circuit

Source: own illustration

Since the parasitics affect the characteristics of components, the C, L, R, D, Q, and other inherent impedance parameter values vary depending on the operating conditions of the components. For real-world measurements, it is understood that the measurement result always contains some error. Some typical error sources are:

- Instrument inaccuracies (including DC bias inaccuracy, test signal level inaccuracy, and impedance measurement inaccuracy)
- Residuals in the test fixture and cables
- Noise

The measurement errors are compensated to reduce the effects of the error sources and are commonly called as de embedding technique. This technique stores the measured value of errors and is de embedded on the program to deduct from the actual measurement. Although this procedure is widely accepted and recognized, there are some factors that may not have been considered which are the environmental factor. A circuit designed to pass a certain frequencies may not be able to perform according to its specification as the impedance of the circuit is no longer in resonant with the assigned frequencies.

In a perfect world, it is known that the transmission zeros appears near the pass band when the parameter S_{21}=0. The even and the odd mode analysis can give the expression of the S_{21} based on the odd- and the even-mode input admittances. The expression of the S_{21} as shown on EQ 2 is given by: (Pozar, 1998)

$$S_{21} = \frac{Y_{in}^{o} Y^{o} - Y_{in}^{e} Y^{o}}{\left(Y_{in}^{o} + Y^{o}\right)\left(Y_{in}^{e} + Y^{o}\right)}$$

EQ (2)

Where Y° represents the characteristic admittance. The condition that ensures the appearance of the transmission zeros can be deduced from the equation (1). Thus, we can write Equation 3 as:

$$Y_{in}^{o}Y^{o} - Y_{in}^{e}Y^{o} = 0$$

EQ (3)

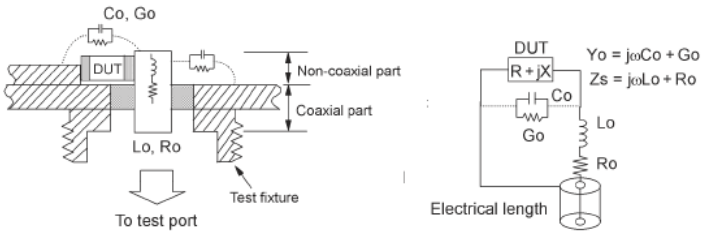
Therefore, this condition can be expressed as:

$$Z\omega C_2\left(\sin 2\theta_1 + \sin 2\theta_2\right) - \cos^2\theta_2 = 0$$

EQ (4)

2.1 How the test fixture and parasitics affects the test performance:

The error source model illustrates a typical test fixture configuration and a model of error sources on Figure 9. The test fixture board is configured specifically with two electrically dissimilar segments: a coaxial connector section and a non-coaxial terminal section for connecting directly to the DUT. On this model, the components were not yet included and will also be discussed on the proceeding topics. The characteristic of the coaxial section is modeled using an equivalent transmission line (distributed constant circuit) and represented by propagation constants. Since the coaxial section is short the propagation loss is neglected, therefore it is assumed that only the phase shift (error) expressed as electrical length exists. The characteristic of the non-coaxial section can be described using the residual impedance and stray admittance model in a two-terminal measurement configuration as shown in Figure 9. The residual impedance (Zs) is assumed to be in series with the DUT and stray admittance (Yo) is in parallel with DUT.



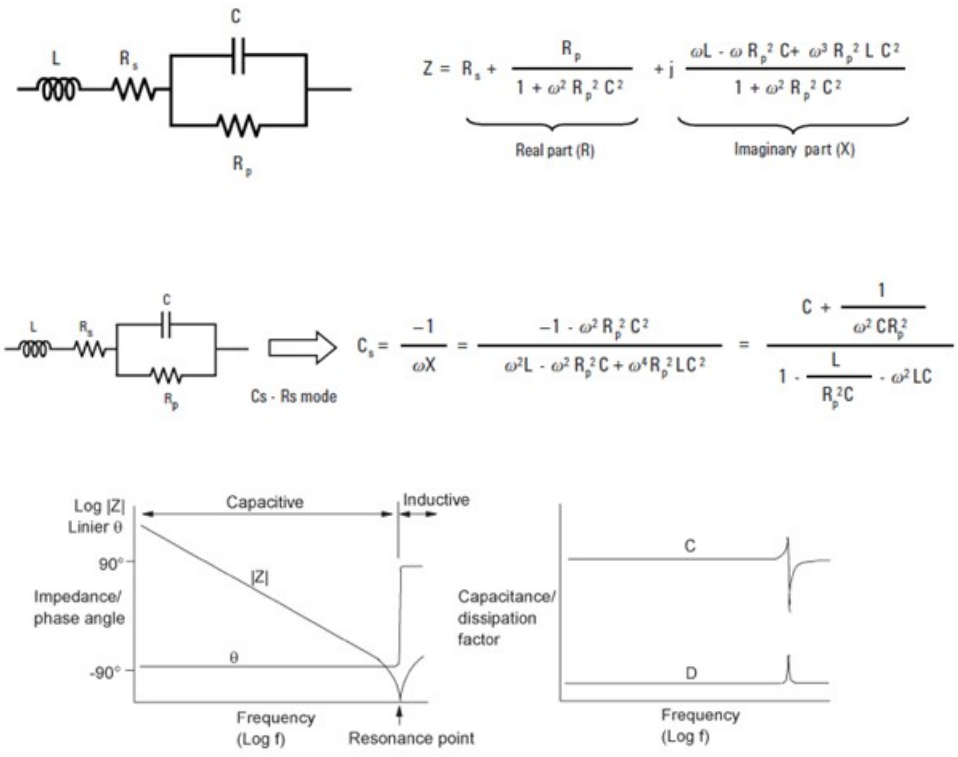
(a) Fixture model (b) Equivalent circuit model

Figure 10 Representation of error source model

Source: (Keysight Technologies, 2016)

The electrical characteristics of the circuit mentioned above would change even more as the effect of added variance in induced thru the presence of the humidity.

Taking a closer look on the effect of humidity on the individual components like capacitors, resistors and inductors, the effective values of these components changes according to the level of humidity present on the components. Figure 11 illustrates the total impedance, Admittance and Susceptance of the circuit changes as well. This deviation on the value of the components deviates even more on the RF parameters and its performance in general.



(a) |Z| - Θ characteristic (b) C – D characteristic

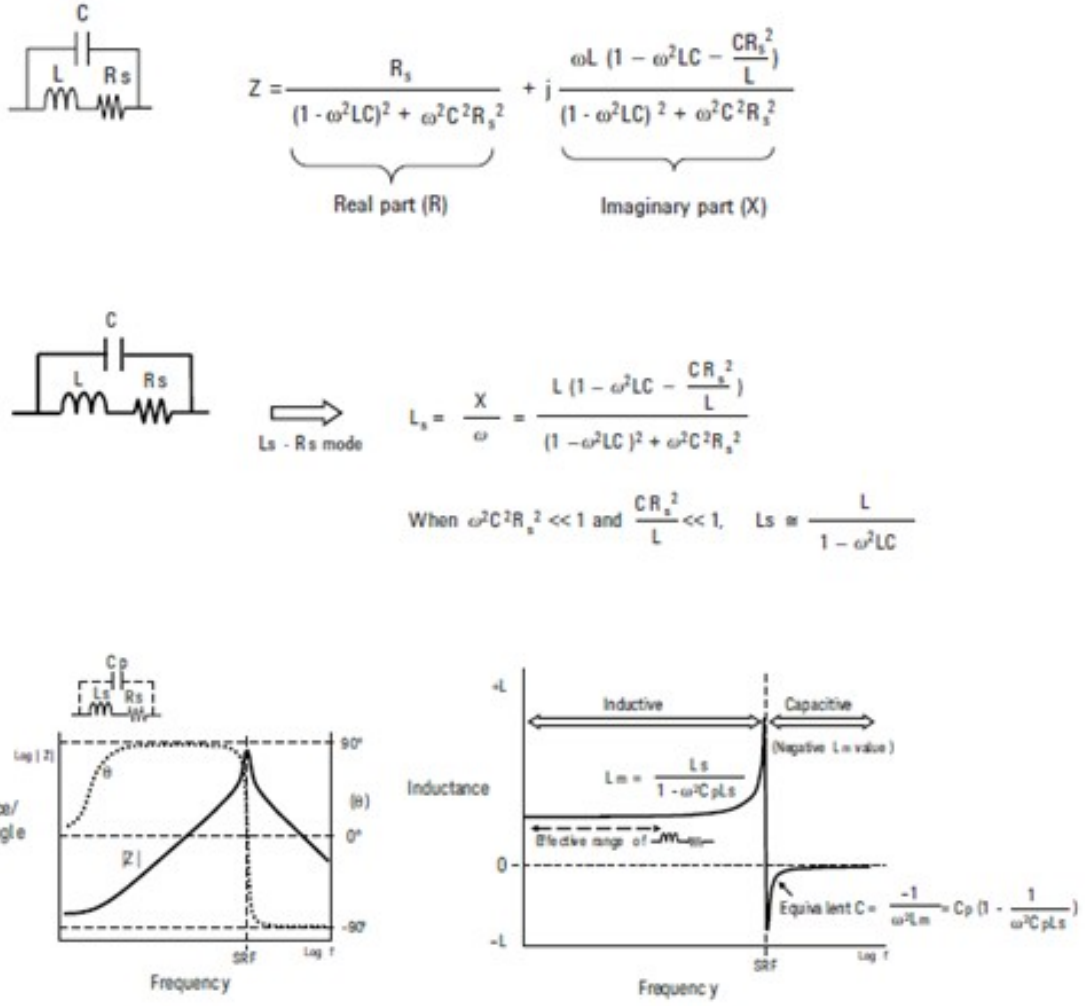
Figure 11 Effects of parasitics on the capacitance measurement

Source: (Keysight Technologies, 2016) , (Alferink, 2014)

A typical equivalent circuit for a capacitor is shown in Figure 11. In this circuit model, C denotes the main element of the capacitor. Rs and L are the residual resistance and inductance existing in the lead wires and electrodes. Rp is a parasitic resistance which

represents the dielectric loss of the dielectric material. The total value of the parasitic components would change according the level of moisture on the circuit.

Since real-world capacitors have complex parasitics, when an impedance measuring instrument measures a lone capacitor in either the series mode (Cs – D or Cs – Rs) or the parallel mode (Cp – D, Cp – G, or Cp – Rp), the displayed capacitance value, Cs or Cp, is not always equal to the real capacitance value, C, of the capacitor. The Rp is usually insignificant and can be disregarded in the cases of high-value capacitors (because Rp >> 1/wC.) For low-value capacitors, the Rp itself has an extremely high value. Therefore, most capacitors can be represented by using a series C-R-L circuit model as shown in Figure 10. Figure 11 (a) and (b) show the typical impedance (|Z| _ q) and Cs – D characteristics of ceramic capacitors, respectively. The existence of L can be recognized from the resonance point seen in the higher frequency region. With regards to the effects of L, it is seen in the higher frequency region where its inductive reactance, wL, is not negligible as shown on Figure 12.



(a) |Z| -Θ frequency response (b) inductance frequency response

Figure12 Effects of parasitics on the inductance measurement

Source (Alferink, 2014), (Keysight Technologies, 2016)

This research paper furthers the study on test fixtures RF characteristics and electrical behavior and thru experiments on the effect of the humidity on the test fixtures to tester mismatch and how it affects the measurement on final test set up through the observable measurement that would greatly benefit product and equipment engineers and production management as this directly affects the equipment availability of the ATE.

3 Methodologies

3.1 Test Set up and testing procedure

The experiments or research conducted on this study are the implements to substantiate the significant effect of environmental factors on the RF performance.

The first experiment investigates the RF Power behavior to the adjacent pins or circuits. And the second experiment utilizes RF scattering parameters to evaluate the effects on the specific and vulnerable socket pins.

For the first experiment, in order to determine the external factor effects on the RF parametric measurement, a bench tester will be set up. A fixture that is presently subjected to the humidity will be used for the primary evaluation activity. Below is the procedure that will be followed:

1. The RF test fixture that will be used for the experiment will be placed on top of a “12 inches “non-conductive engineering plastic acrylonitrile butadiene styrene (ABS) as illustrated on Figure 19.

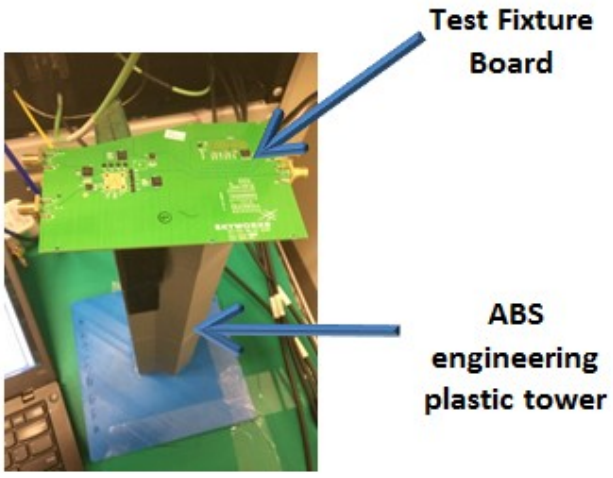


Figure 19 Proposed Test Fixture Mounted on top of the ABS Insulator

Source: own illustration

The reason why the test fixture under test has to be on top of the 12-inch tower engineering plastic is to isolate the fixture from the other ground planes including the electrostatic sensitive device (ESD) table mat table.

2. A 50 Ohms RF cable will be installed on the three RF instruments that will be utilized on this experiment. The other end of the cables this is where the 50 Ohms SMA connector will be mounted. The three RF instruments that will be utilized are: N9020A MXA Signal Analyzer, N5182A MXG Vector Signal Generator, and the E5071C ENA Vector Network Analyzer.

3. The network analyzer frequency sweep will be set to the following configurations:

a. Start Frequency - 750 MHz

b. Stop Frequency – 4.7 GHz

c. IFBW – 70 KHz

And also the Marker/ analysis frequencies settings are shown on Table 3.1 where the assigned frequency are Marked for analysis and evaluation. The power level on these frequencies are captured and displayed on the screen of the Signal Analyzer for fast analysis of the data.

Table 3.1 the Frequency Marker - Analysis

Source: own elaboration

No.	Frequency Setting
1	850 MHz
2	1.7 GHz
3	2.0 GHz
4	2.4 GHz
5	2.7 GHz
6	3.0 GHz
7	3.2 GHz

8	3.4 GHz
9	3.7 GHz

4. A Test Points will be assigned on the socket pads on the fixture where the test RF Measurements will be taken. These test points will be the reference points where all the necessary information that will be available will be collected. Figure 20 shows and indicates the location of the test points on the fixture board.

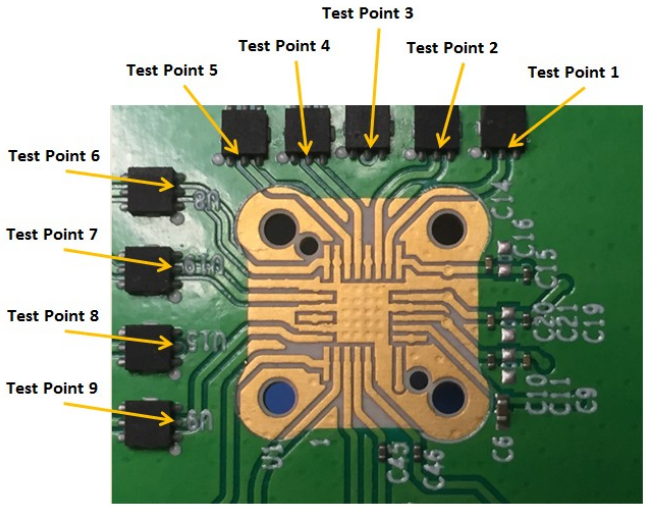


Figure 20 Test Fixture Socket Pad with Assigned Test Points

Source: own illustration

5. N5182A MXG Vector Signal Generator power output level will be set to 0 dBm and the frequencies to be used are the same settings on the network analyzer.

6. The N9020A MXA Signal Analyzer center frequencies and markers are the same as the settings of the E5071C ENA Vector Network Analyzer.

7. Whenever the signal generator frequencies are changed, the signal analyzer center frequency and marker are also changed accordingly.

8. The output cable of the signal generator with its RF frequency setting set to 850 MHz; introduce the other end of the same cable with SMA end connector on

the ground center pad of the printed circuit board (PCB). Turn the switches on of the CW, Modulated signal and the RF switches of the signal generator.

9. Using the signal analyzer with the center frequency and marker setting set to 850 MHz; measure the power levels on each of the test points by introducing the cable with SMA end connector to every test points. Record and save the measured power level.

10. For other frequency responses, data will be collected by repeating procedure 8 and 9 following the frequency and marker settings on procedure 3.

11. Taking RF measurement using the network analyzer, the RF cables are mounted on the Port 1and Port 2 of the instrument and the other ends of the cables with SMA connector will used to introduce the force and measure signals on the socket pads. S11 and S22 scattering parameters will be measured across all of the test points with one connector, the source and later the measure will be on the ground center pad.

12. The same test fixture will be subjected to bake process to remove the humidity on the surface of the fixture for 30 to 40 mins at temperature of 65 to 75 Degrees Centigrade.

13. Store the fixture board in a sealed plastic bag with desiccant and humidity sensor until the temperature on the board has stabilized. The procedure 1 to 11 will be repeated but this time it will be for the humidity free board. The second experiment is for the board that has undergone cleaning process, drying well and baked in the oven for 30 minutes at temperature of 65 Deg. Centigrade as described on the recommendations of this paper.

3.2 Required Resources

The following instruments and materials illustrated below were used in the accomplishment of the experiments on this study.

1. A 50 Ohms RF cable as illustrated on Figure 21 will be installed and calibrated on the RF instruments MXA Signal Analyzer N9020A, MXG Vector Signal Generator N5182A and ENA Vector Network Analyzer E5071C. Figure 14 shows the low loss 50 Ohms RF cable with an SMA male connector on one end and an SMA female connector on another end.

Figure 21 a 50 Ohms RF cable

Source: (EC Microwave, 2018)

2. A 50 Ohms female SMA edge connector will be placed on the other end of the RF cables and will be used as the test pin tip. As shown on Figure 22 having a threaded interface, SMA 50 Ohm connectors are semi-precision units that provide excellent electrical performance from DC to 26.5 GHz and outstanding mechanical durability.

Figure 22 a subminiature version A (SMA) Female connector

Source: own illustration

3. Figure 23 is an N9020A MXA Signal Analyzer, 10 Hz to 13.6 GHz – this spectrum analyzer will be used measure the magnitude of an input signal versus frequency within the identified frequency on each pad of the RF test fixture. The primary goal is to measure the power of the assigned spectrum of known and unknown frequencies on the designated socket pad pins.

Figure 23 N9020A MXA Signal Analyzer

Source: (Keysight Technologies, 2000-2018)

4. N5182A MXG Vector Signal Generator, 100 kHz to 6 GHz – the RF signal generator will be used as a source for the RF frequencies that will be injected on the test fixture. As illustrated on Figure 24, a Vector signal generators typically incorporate a high end RF signal generator with an IQ modulator. In addition to this, they often include an arbitrary waveform generator in one form or another. This is used to generate the complicated baseband modulation signals required to modulate the RF signal.

Figure 24 N5182A MXG Vector Signal Generator

Source: (Keysight Technologies, 2000-2018)

5. E5071C 300 KHz -20 GHz ENA Vector Network Analyzer – will be used generate a signal and analyze the test fixture by measuring the s-parameter (scattering parameters) because of the transmission and reflection of the signal. As illustrated on Figure 25, a network analyzer (also called a protocol analyzer or packet analyzer) is a combination of hardware and exclusive programs.

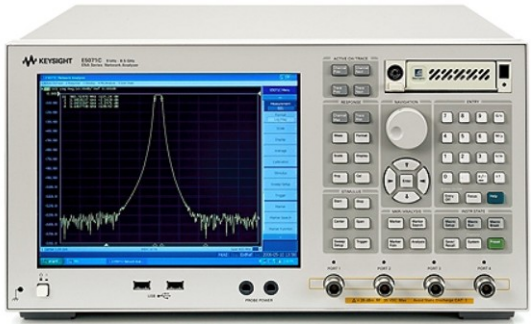


Figure 25 E5071C ENA Vector Network Analyzer

Source: (Keysight Technologies, 2000-2018)

6. Desiccant – will be used to effectively keep the moisture formation on the RF test fixture due to humidity. As shown on Figure 26, the desiccant works by a process called *adsorption*. The water in the air actually absorbs between the tiny passages as the air passes through them. The water molecules become trapped so that the air is dried out as it passes

through the filter. This process is reversible. If the silica gel desiccant is heated to ~180°F, it will release the trapped water. This process is called *regenerating* the desiccant (DryTech Inc., 2018).

Figure 26 Desiccant

Source: (DryTech Inc., 2018)

7. Humidity indicator – will be used to quantify relative humidity in a sealed packaging where the RF test fixture will be enclosed for experiment. As illustrated on Figure 27. Humidity Indicator Cards tell at a glance if moisture within sealed containers or closed spaces is at an acceptable level. Cobalt-free cards do not contain heavy metals. These cards help monitor desiccant activity and are ideal for use with desiccants in any application where moisture control is critical. Any color change from blue to pink (cobalt cards) or brown to green (cobalt-free cards) indicates an unsealed container and/or damaging level of humidity. Has indicating element calibrated for a permanent accuracy of ±5% of relative humidity in each application (Sigma-Aldrich, 2018).

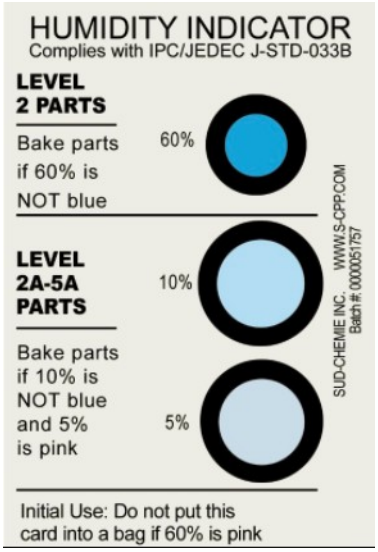


Figure 27 Humidity Indicator

Source: own illustration

8. Ultrasonic Cleaner – Figure 28 is an ultrasonic baths with self-adaptive technology that provides industry-leading cleaning quality. This ultrasonic bath will be used to soak the newly repaired or assembled fixture board to remove the flux residues.

Figure 28 Ultrasonic Bath

Source: (Branson)

9. Temperature Chamber – Figure 29 is an environmental chamber, also called a climatic chamber or climate chamber. It is an enclosure used to test the effects of specified environmental conditions in industrial products, materials, and electronic devices and components. On this experiment, this temperature chamber is used to remove the humidity on the surface and on every component parts of the fixture.

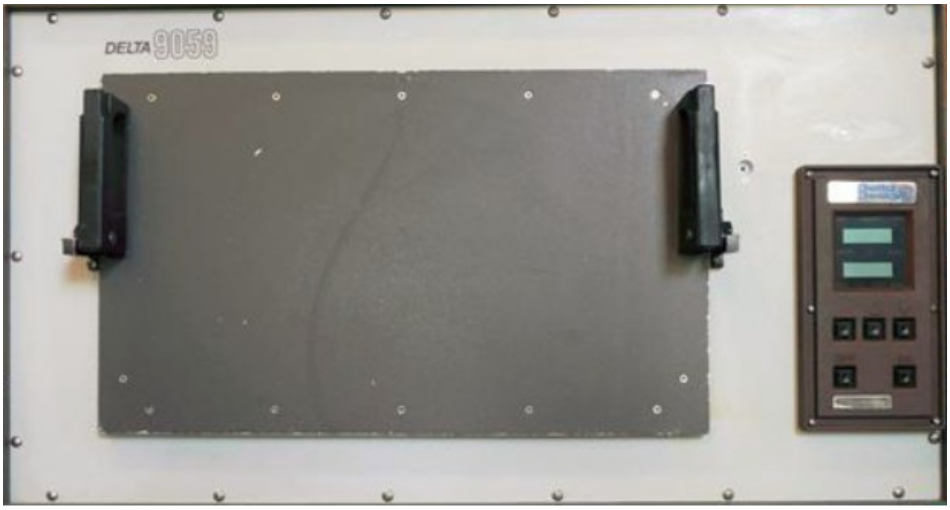


Figure 29 Temperature Chamber

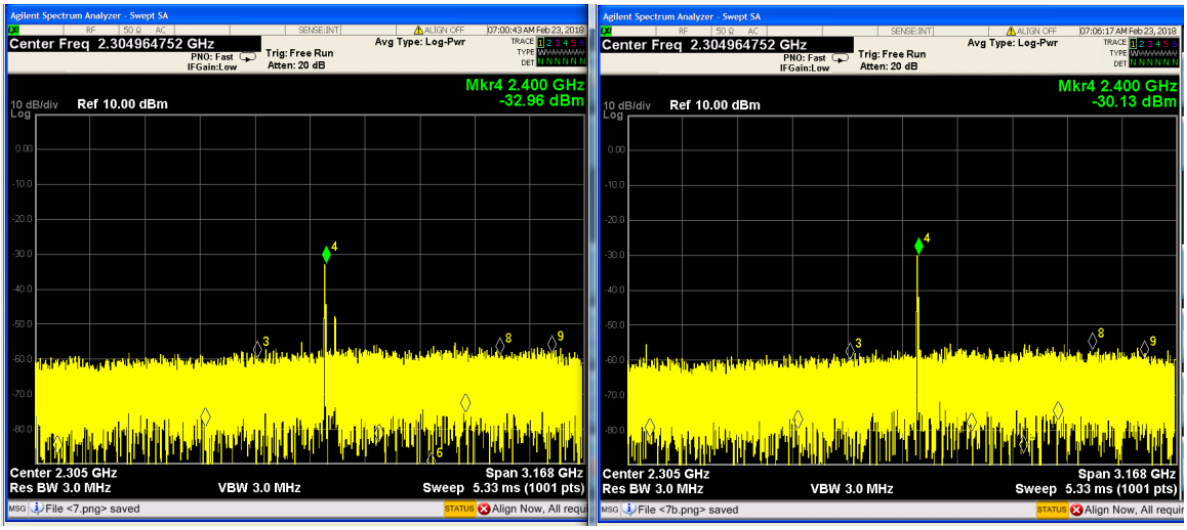
Source: (COHU Delta Design)

4 Results

The proposed process method as indicated on the recommendation was performed on the fixture after the first measurement with humidity was conducted. The result of the experimentation on the fixtures reveals how the parasitic components have deviated significantly from its original value. It can also be seen that some measurement points and indicated frequencies may not have expressively reflected a noteworthy effect.

Based on the first experiments, The RF power injection on the circuit and measure on the adjacent pins shows how the effective measured value changes depends on frequencies, power level, devalued parasitic components.

On the image shown on Figure 30, the measurement is taken at Point 9 (P9) at the center frequency 2.4 GHz. The reference power level is 10 dBm having a frequency span of 3.2 GHz. The horizontal indicator is the frequency range of the spectrum which is 800 MHz to 4 GHz considered on this study. The vertical indicator is the power level that was referenced to the 10 dBm.



(a) Measured at 8-15% humidity (b) measured at 3-6% humidity

Figure 30 Power measured on P9 @ 2.4 GHz frequency (a) before the process method (b) after the new process method

Source: own illustration, using N9020A MXA Signal Analyzer

The power level was measured on the Pin 9 for both condition of the board where:

(a) The board was in original condition where fluxes with humidity is present on the surface of the board and

(b) The processed condition where the board is free of humidity. The fixture board was subjected to the process as indicated on the recommendations of this study.

A Power level 0dBm at center frequency of 2.4 GHz was injected on the Ground point which is at the center of the socket pin and the power level measurement was taken on the adjacent pin and this test point Pin 9 as indicated on Table 5.1.

Figure 30 (a) shows that the power level measured on adjacent pin 9 with the board at original condition is -32.96 dBm

Figure 30 (b) shows the power level on adjacent pin P9 after the board was subjected to the new process method is -30.13 dBm a delta of 1.83 dBm power.

A substantial amount of power change on the same pin was observed. This power deviation in power will be amplified in the ATE system once the DC power and the DUT is installed and the final test de embedding and embedding if performed during qualification run.

Another significant finding is illustrated on Figure 31 where it reveals a significant variation in power levels after the fixture was subjected to the new process method. It has been observed that a deviation in power of 11.09 dBm signifies a great potential of error source when the fixture is installed in the system where the signal will be amplified in the process.

The power level measurement was taken on the Pin 2 for both condition of the board where:

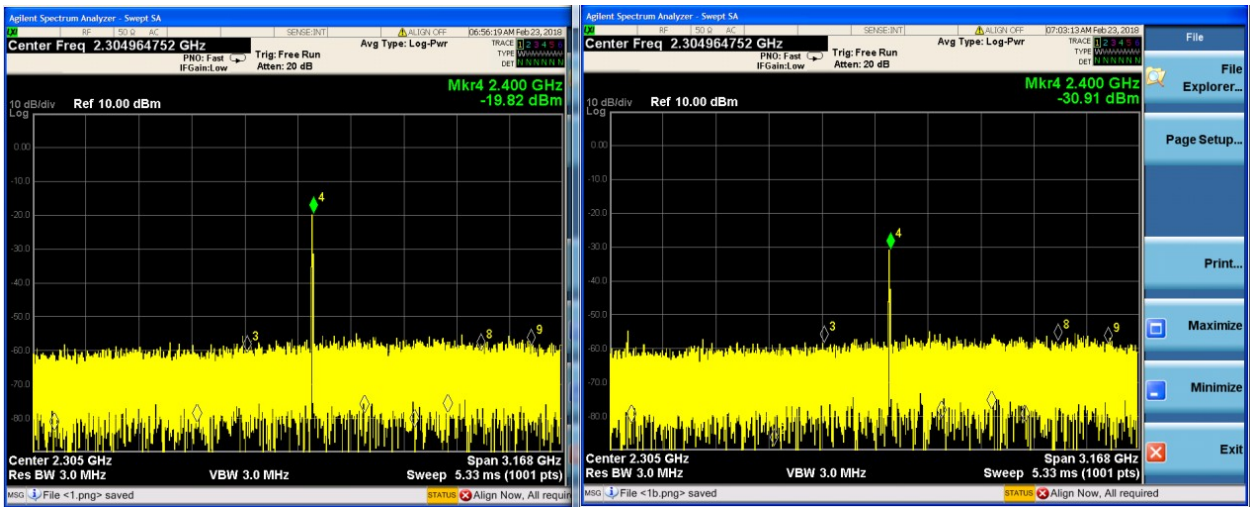
(a) The board was in original condition where fluxes with humidity is present on the surface of the board and

(b) The processed condition where the board is free of humidity. The fixture board was subjected to the process as indicated on the recommendations of this study.

A Power level 0dBm with a center frequency of 2.4 GHz was injected on the Ground point which is at the center of the socket pin and the power level measurement was taken on the adjacent pin and this test point is Pin 2 as indicated on Table 5.1.

Figure 31 (a) shows that the power level measured on adjacent pin 9 with the board at original condition is -19.82 dBm

Figure 31 (b) shows the power level on adjacent pin P9 after the board was subjected to the new process method is -30.91 dBm a delta of 11.09 dBm power.



(a) Measured at 8-15% humidity (b) Measured at 3-6% humidity

Figure 31 Power measured on P2 @ 2.4 GHz frequency (a) before the process method (b) after the process method

Source: own illustration, using N9020A MXA Signal Analyzer

And yet another part of the experiment using the first experiment method is the variation in the center frequency which at this time the frequency is 3.4 GHZ. The measured power level at Pin 2 reveals an imperative level of power changes after the fixture was subjected to the new process method. This again could create an impact when this fixture is utilized on the system with uncontrolled parasitic values on the fixture that may cause a tester to tester mismatch as described on the problem statement. If the fixture was subjected to the de-embedded and embedding process where the parasitics and other losses were taken into account, the fixtures' parasitic values may vary yet uncontrollably when temperature changes and the effect of humidity was not eliminated earlier.

Another experiment was conducted where measurement was taken at Pin P5 at center frequency of 3.4 GHz as shown of Figure 32.

The power level measurement was taken on the Pin 5 for both condition of the board where:

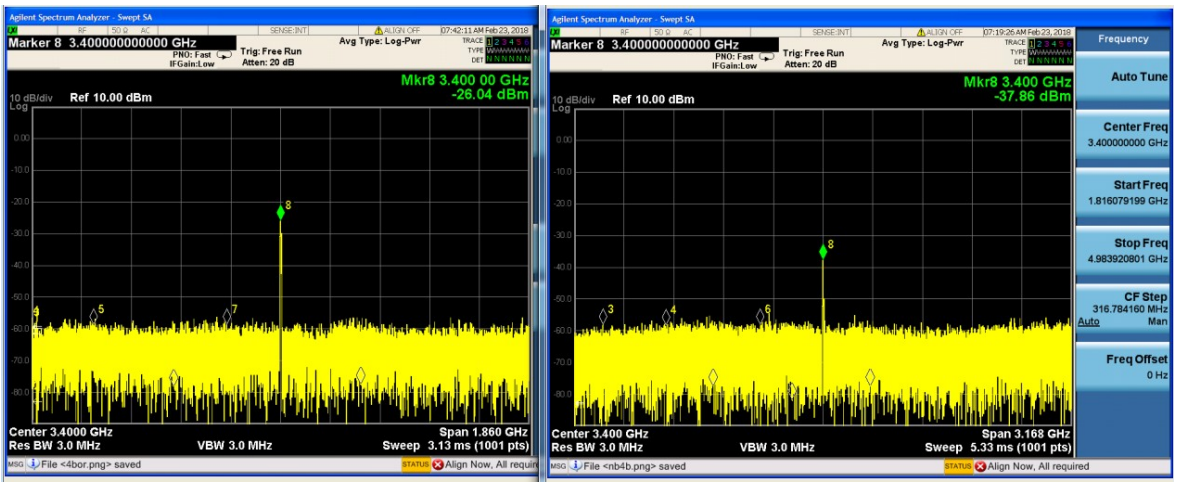
(a) The board was in original condition where fluxes with humidity is present on the surface of the board and

(b) The processed condition where the board is free of humidity. The fixture board was subjected to the process as indicated on the recommendations of this study.

A Power level 0dBm with a center frequency of 3.4 GHz was injected on the Ground point which is at the center of the socket pin and the power level measurement was taken on the adjacent pin and this test point is Pin 5 as indicated on Table 5.1.

Figure 32 (a) shows that the power level measured on adjacent pin 9 with the board at original condition is -26.04 dBm

Figure 32 (b) shows the power level on adjacent pin P9 after the board was subjected to the new process method is -37.86 dBm a delta of 11.82 dBm power.



(a) Measured at 8-15% humidity (b) Measured at 3-6% humidity

Figure 32 Power measured on P5 @ 3.4 GHz frequency (a) before the process method (b) after the process method

Source: own illustration, using N9020A MXA Signal Analyzer

A deviation of 11.82 dBm was observed. This amount of delta in measurement if this same pin and frequency is used during the final test, this may contribute to the deviation in the RF performance of the fixture.

As for the summary of the first experiment, the power deviation detected on the socket pins was measured while the fixture board was in original condition where in the fixture has the presence of flux residues and humidity has resided on it. As illustrated on Table 4.1, the power level measurement was compared to the same fixture after it was subjected to the proposed method of cleaning and dehumidification. The first row of the table indicates the frequencies of as the focus of this study, the second column is the socket pins of the fixture where the signal power will be measured, and the third and fourth columns were the measurement taken before and after the board was subjected to the new proposed process method. The last column of the table is the delta or the difference in measurements of the board. The rows where are the center frequencies where the measurements was based upon.

Table 4.1 Power Level Delta per Socket Pins

Source: own elaboration

Frequency	Socket Pins	Power @ Original condition (dBm)	Power after new method (dBm)	Delta
850 MHz	P1	-14.84	-15.97	1.13
	P2	-14.73	-14.27	-0.46
	P4	-18.07	-18.16	0.09
	P5	-21.8	-21.02	-0.78
	P6	-18.55	-20.37	1.82
	P7	-19.91	-22.53	2.62
	P9	-19.81	-17.21	-2.6
2.4 GHz	P1	-30.47	-28.62	-1.85
	P2	-19.82	-30.91	11.09
	P4	-35.11	-33.99	-1.12
	P5	-33.09	-33.91	0.82
	P6	-35.56	-32.99	-2.57
	P7	-31.89	-32.7	0.81
	P9	-32.96	-30.13	-2.83
3.4 GHz	P1	-18.89	-18.63	-0.26
	P2	-24.98	-29.01	4.03
	P4	-21.92	-32.2	10.28
	P5	-26.04	-37.86	11.82
	P6	-27.18	-22.49	-4.69
	P7	-16.64	-27.54	10.9
	P9	-15.98	-23.83	7.85

The second experiment uses a Network Analyzer to scrutinize the signal power levels on the assigned sweep frequencies. The scattering parameters S11 and S22 were used and were set to measure on Site1 and Site 2 fixture boards. The information that was derived from this research shows significant evidence how the impedance of a circuit is affected by the parasitic components that have deviated from the effective measurements due to the humidity factor.

The reflection method was also used in this study as familiarity and ease to understand takes its place. Using the familiar scattering parameters (S-parameters) from vector network analysis, the reflection method derives impedance values from S11 for site 1

and S22 for site 2 as shown on Figure 33. It can be observed that site 1 (yellow colored plot) has deviated on the frequencies 1.7 GHz to 2.1 GHz range. Also the site 2 swept frequencies has lowered from its original reference position thereby both plots have intersected on some frequencies. For this reason, the effect of humidity on the board is translated to the scattering parameters. This is further enhanced when the fixture is installed on the system where more RF components could interact with the fixtures' off set parameters. The dilemma begins when the de-embedding procedure is performed during qualification activities with an undetected offset from the fixture; this offset will also be included as compensation measurement for embedding process. And when the board's humidity on the surface changes due to the temperature of the testers and surrounding, the effect would again deviate and this would again introduce a variation on the tester measurements. Thereby causing a tester to tester mismatch problem as stated on the problem statement of this study.

The network analyzer parameters indicators are described below:

a. Vertical indicators: reflects the power level and the reference power

b. Horizontal indicators: the frequency sweeps with a Start Frequency of 300 KHz and End Frequency of 3 GHz

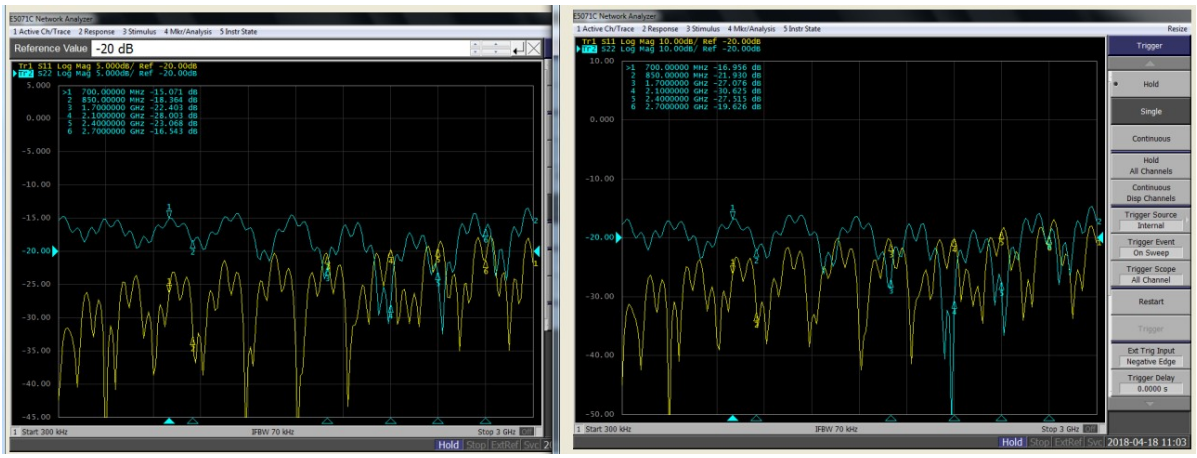
c. Intermediate Frequency Bandwidth (IFBW) of 70 KHz.

d. The Marker Settings is shown on Table 4.2

Table 4.2 Frequency Marker Settings

Source: own elaboration

Marker Set	Marked Frequency
1	700 MHz
2	850 MHz
3	1.7 GHz
4	2.1 GHz
5	2.4 GHz
6	2.7 GHz

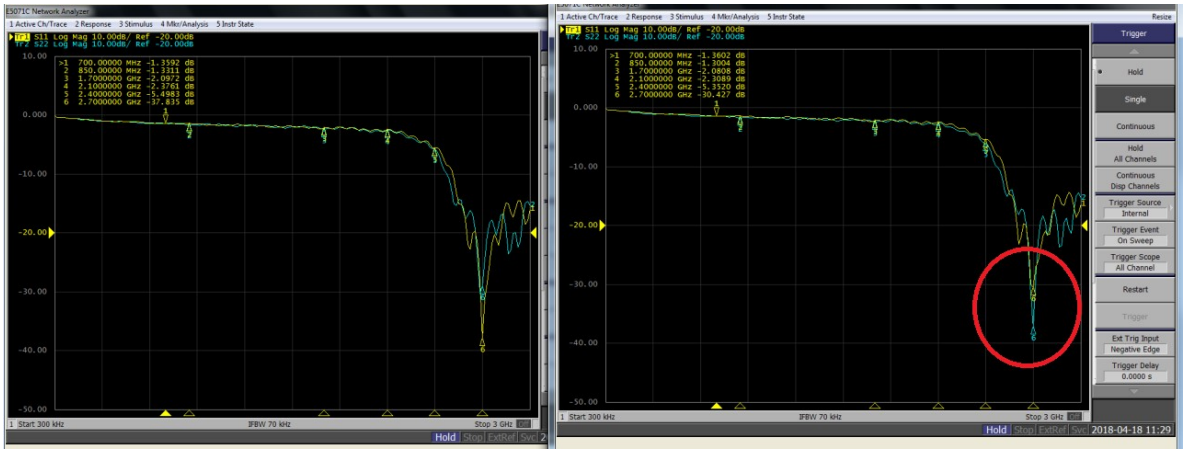


(a) Measured at 8-15% humidity (b) Measured at 3-6% humidity

Figure 33 Frequency swept at J3 RX COM port (a) before the process method (b) after the process method

Source: own illustration*, using* E5071C ENA Vector Network Analyzer

As illustrated on Figure 34, it can be observed that site 2 has little effect as to when the fixture board was subjected to the new process of cleaning specifically at 2.7 GHz frequency. This is most likely because the humidified fluxes on the fixture are not on the area where J5 is positioned.

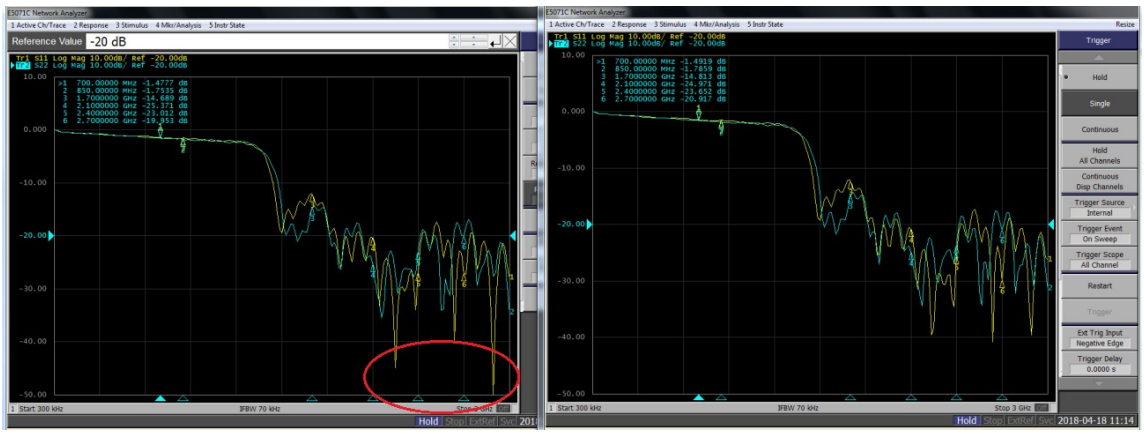


(a) Measured at 8-15% humidity (b) Measured at 3-6% humidity

Figure 34 Frequency swept at J5 HB HRM OUT port (a) before the process method (b) after the process method

Source: own illustration*, using* E5071C ENA Vector Network Analyzer

Figure 35 exhibits the same result and also falls on the same category as J5 with a significant effects on specific frequencies only.



(a) Measured at 8-15% humidity (b) Measured at 3-6% humidity

Figure 35 Frequency swept at J6 LB HRM OUT port (a) before the process method (b) after the process method

Source: own illustration*, using* E5071C ENA Vector Network Analyzer

Figure 36, reveals the Harmonic Output pins reflections that have a difference in measurement between sites considering both sites have different level of humidity on the surfaces. The circuit impedance changes and the circuit are no longer in 50 Ohms or close to it as it is designed originally.

Figure 36 Site 1(S11) and Site 2 (S22) scattering parameters measured at J6 LB HRM OUT point

Source: own illustration, Using Keysight E5071C ENA Vector Network Analyzer

Figure 37 demonstrate the Scattering parameters that are measured on both Sites of the fixture boards 1 and 2 were not significantly affected by humidity for the reason that on these output pins circuitry there is less or no humidity on the surface.

Figure 37 Site 1- S11and S2 - S22 scattering parameters measured at J5 HB HRM OUT point

Source: own illustration, Using Keysight E5071C ENA Vector Network Analyzer

There are also part of the fixture that there are only specific frequency that is affected. This is due to the impedance of the circuit affected may have affected only the specific frequency by any chance. Figure 38 shows that in between the frequencies 850 MHz and 1.7 GHz Site 2 has significant loss while on the other bands Site 1 has greater loss.

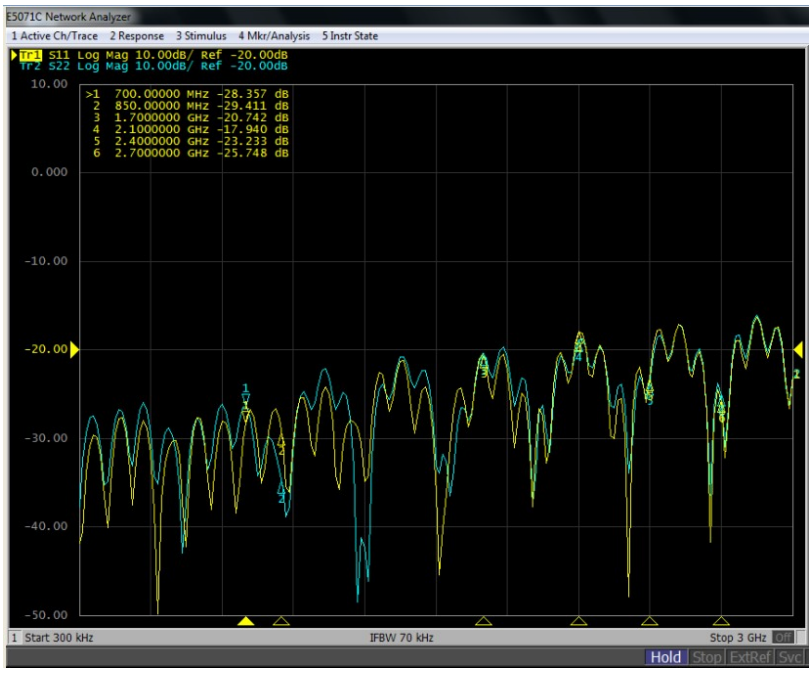


Figure 38 Site 1- S11and S2 - S22 scattering parameters measured at J4 Ant point

Source: own illustration, Using Keysight E5071C ENA Vector Network Analyzer

5 Recommendations

A new process method is proposed: this new procedure will exclude and eliminate the effects of environmental factor such as humidity on the test fixtures that cause a mismatch issue during production set up. A properly cleaned fixture board leaves no chance for the component parasitics to deviate from the previous measurement that was taken during verification and qualification process.

5.1 Cleaning procedure before storage

a. Place the Fixture PCB board in the ultrasonic cleaner for 15 to 30 minutes as illustrated on Figure 39, where the fixture boards are soaked under the cleaning solution to unstiffen the dried and sturdy fluxes and its residues.

Figure 39 Ultrasonic cleaner (Branson brand)

Source: (Branson)

b. Clean the Fixture PCB board in the ultrasonic cleaner using soft bristle brush as illustrated on Figure 40. Completely removing any flux residues on the surface of the PCB, on every pins and corners of the components, and on the VIAS. This will prevent the moisture to settle and absorbed by the flux residue as shown on Figures 2, 3 and 4. The brush used on this cleaning procedure is a wooden handle and the bristles are made of stringed soft polymer plastics.

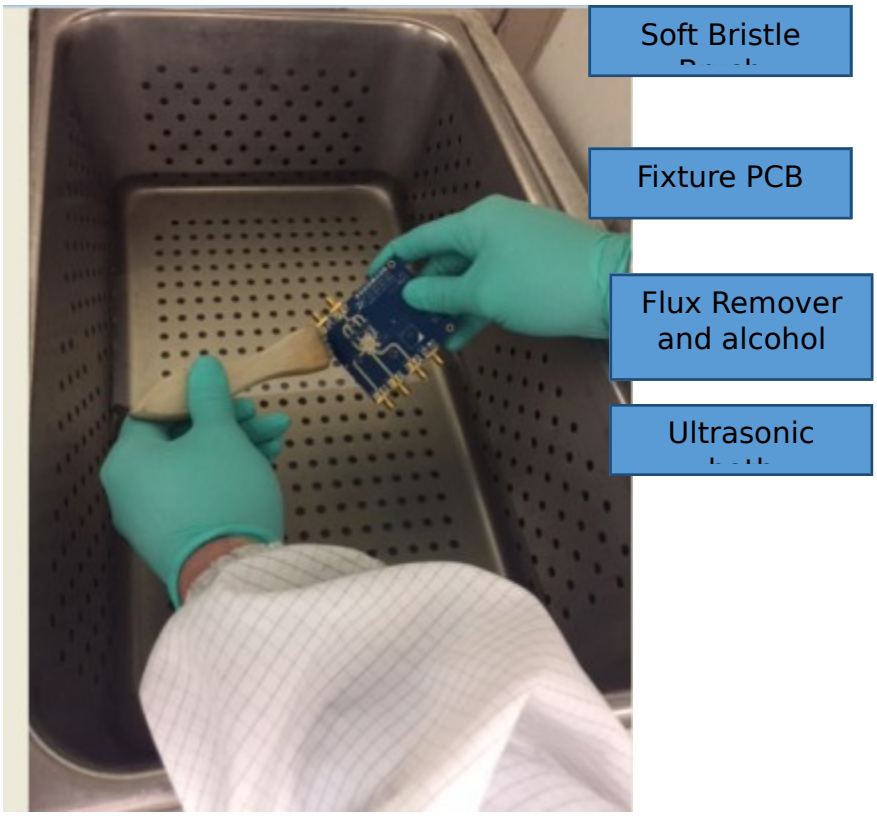


Figure 40 Board being brushed while immersed in alcohol (IPA)

Source: own illustration

c. Completely dry the fixture with a compressed dry Air (CDA). As shown on Figure 41, the air pistol (blue) is manually controlled by the user thru the exertion of gripping force. The compressed dry air with high pressure is released on the nozzle in proportion to the force that the air pistol is pressed by the user. Dry the fixture

thoroughly focusing the nozzle of the pistol on the corners and under of the components and VIAS.

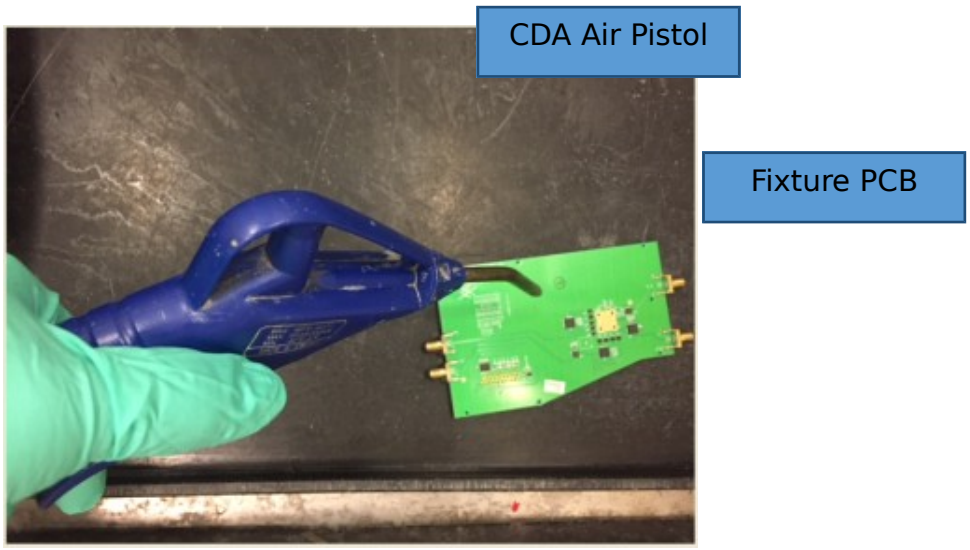


Figure 41 Board being dried using the compressed dry air

Source: own illustration

d. To remove the moist or to de-humidify the fixture, bake the board for 30 minutes at temperature of 65°C to 70°C as shown on Figure 42. If no bake oven is available, a hot air gun can be used. The heat has to be applied equally on all the surface of the board drying completely all the components and the surface of the board.

Figure 42 Board being dried in an oven

Source: own illustration

e. Store back the fixture on the assigned enclosure with a moisture indicator and large sized desiccants. Figure 43 shows the test fixture inside the tight sealed thermoplastic polymer (ABS) enclosure. The fixture is deposited in a polymer enclosure with desiccants as illustrated on Figure 19 strategically placed side by side for each of the fixture test site and a humidity indicator placed inside the enclosure as shown on Figure 43.

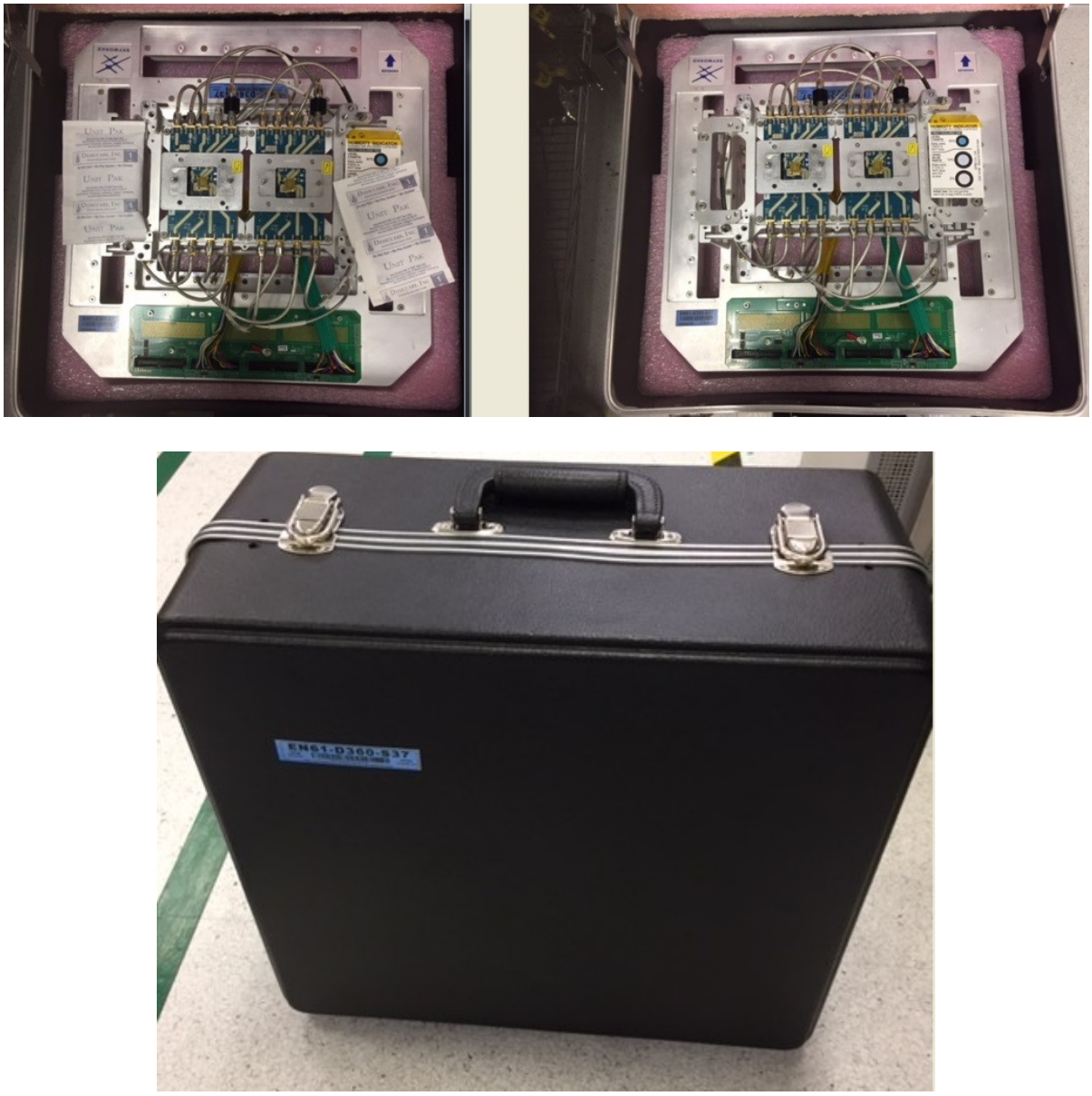


Figure 43 Board stored inside the enclosure with humidity sensor and desiccants

Source: own illustration

5.2 Procedure before using the fixture from storage

a. Check the humidity level indicator color

If 5 % is pink and the 10% is not completely blue - bake the fixture for 30 minutes at 65°C – 70 °C or de-humidify using the controlled temperature heat gun on the entire board and edges of the connectors.

6 Discussions and Conclusion

When a measurement is affected only by component residuals, the effective value can be corrected by simply subtracting the error value from the measured value. Two approaches have been developed for removing the effects of the test fixture from the measurement, which fall into two fundamental categories: direct measurement and de-embedding (Agilent Technologies, 2001, 2004). These two approaches provide accurate measurement in the DUT test. Unfortunately these approaches do not allow for real-time feedback to the operator because the measured data needs to be captured and post-processed in order to remove the effects of the un-accounted residuals in the test fixture. Such that when the fixture was again utilized but this time with the added error contributed by the residuals from fluxes and humidity that settled on it, the fixture will reflects the new parasitic' s inherent residuals and inaccuracies (Figure 9). Therefore the processed information will not match to the measured value with the fixture that has different measurement and contain errors when comparison is made. The errors also vary intrinsically from one measurement to another; their differences depend on a multitude of considerations in regard to measurement uncertainties, such as amount of fluxes and humidity it had adsorbed and the temperature. We can judge the quality of measurements by comparing how closely a measured value agrees with the real value under a defined set of measurement conditions. The measured value is what is expected, and the goal of measurement is to have the measured value be as close as possible to the real value without the added effect of the humidity.

The first experiment revealed that the power captured by the adjacent pins varies depending on the amount of fluxes and humidity present on the surface of the fixture. As shown on Table 5.1, the delta readings between the measurement of the fixture for with and without the fluxes and humidity also depends on the frequency as when the measurement was taken. But the information concludes that the measured value of has changed significantly though it may not be the same on all frequency range.

On the second experiment conducted, it is evident how these impurities affect the RF performance. Scattering parameters S11 and S22 that were taken on both sites 1 and 2 of the Test Fixture reveals how the reflections through Impedance mismatch occurs. The Value of the scattering parameters varies depends on the amount of fluxes and or humidity that is settled on the surface of the fixture and on the components.

It is therefore necessary to implement the recommended process method on every test fixture. The research study provided essential information regarding the effect of the environmental factors on the RF performance. Carrying out the new process method would simply mean eliminating the un-controlled parasitics on the circuit and thereby eliminating the errors induced that causes a fixture mismatch.

References

(n.d.).

Agilent Technologies. (2001, 2004, May 30). Agilent De-embedding and Embedding S-Parameter Networks Using a Vector Network Analyzer. *Application Note 1364-1*. doi:5980-2784EN

Alferink, F. (2014, June 9). *meettechniek.info*. Retrieved from meettechniek.info: https://meettechniek.info/passive/parasitic.html

Balanis, C. A. (2016). *Antenna theory: analysis and design 4th edition.* United States: John Wiley & Sons.

Balanis, C. A. (2016). *Antenna theory: analysis and design.* John Wiley & Sons.

Branson. (n.d.). *bransonic.com*. Retrieved from www.bransonic.com: https://www.bransonic.com/

COHU Delta Design. (n.d.). *cohu.com*. Retrieved from cohu.com: http://www.cohu.com

DryTech Inc. (2018). *drytechinc.com*. Retrieved from drytechinc.com: https://www.drytechinc.com

EC Microwave. (2018). *ecmicrowave.com*. Retrieved from ecmicrowave.com: http://www.ecmicrowave.com

Fawley, R., & Ferrie, P. (2012). The effects of moisture on the performance of a highly sensitive microwave transmission line frequency descriminator. *Passive RF and Microwave Components, 3rd Annual Seminar.* London: IET. doi:10.1049/ic.2012.0066

Fukunaga, K., & Kurahashi, S. (2007). Dielectric Properties of Printed Circuit Board Insulations at Microwaves and Millimetre Waves. *International Conference on Electromagnetics in Advanced Applications, 2007. ICEAA 2007.* Torino, Italy: IEEE. doi:10.1109/ICEAA.2007.4387305

Hickman, I. (2006). *RF Handbook 4th Edition.* Newnes.

Janas, E., Czuba, K., Mavric, U., & Schlarb, H. (2016). Temperature and Humidity Drift Characterization of Passive RF Components for a Two-Tone Calibration Method. *ISBN 978-3-95450-177-9*.

Keysight Technologies. (2000-2018). *Keysight Technologies*. Retrieved from Keysight Technologies: https://www.keysight.com/en/pdx-x202266-pn-N9020A/mxa-signal-analyzer-10-hz-to-265-ghz?cc=MX&lc=eng

Keysight Technologies. (2000-2018). *Keysight Technologies*. Retrieved from Keysight Technologies: https://www.keysight.com/en/pd-797248-pn-N5182A/mxg-rf-vector-signal-generator?cc=US&lc=eng

Keysight Technologies. (2000-2018). *Keysight Technologies*. Retrieved from Keysight Technologies: https://www.keysight.com/en/pdx-x202270-pn-E5071C/ena-vector-network-analyzer?cc=US&lc=eng&state=2

Keysight Technologies. (2015). Fundamentals of RF and Microwave Noise Figure Measurements - Application Note. *Application Notes*.

Keysight Technologies. (2016, November 2). Impedance Measurement Handbook, Aguide to measurement technology and techniques, 6th edition, Application Note. US: Keysight Technologies.

Li , L., Jun, F., Jingnan, P., Chulsoon , H., Gyuyeong, C., Harkbyeong, P., & Yaojiang, Z. (2015). "Measurement validation for radio-frequency interference estimation by reciprocity theorem. *Electromagnetic Compatibility* , (pp. 154-159).

Litvak, B. K. (2011). Noise Versus Coherency in MM-Wave and Microwave Scattering from Inhomogeneous Materials. *Progress in Electromagnetic Research B, Vol. 28*, pp. 35-54.

LTXC. (2018). Retrieved from LTXC Tester Group of Excerra: http://ltxc.com/

Pan, J., Li, L., Gao, X., & Fan, J. (2015). Application of dipole-moment model in EMI estimation. *2015 IEEE International Symposium on Electromagnetic Compatibility and EMC Europe* (pp. 350 - 354). Dresden: IEEE.

Poole, I. (2012). Electronic / RF Noise Measurement. *RF Technology and Design*.

Pozar, D. M. (1998). *Microwave Engineering.* John Wiley & Sons.

Sigma-Aldrich. (2018). *sigmaaldrich*. Retrieved from sigmaaldrich.com: https://www.sigmaaldrich.com

Society of Cable and Telecomunications Engineers. (2011). *Measurement Procedure for Noise Power Ratio.* Exton, PA: SCTE, Inc.

Timiri, S. (1997). RF Interference Analysis for Collocated Systems. *Microwave Journal*.

Wilson, P. (1995). On correlating TEM cell and OATS emission measurements. *Electromagnetic Compatibility, IEEE Transactions on 37*, (pp. 1-16).

Xin, T., Nothofer, T. A., Sewell, P., & Christopoulos, C. (2010). A genetic algorithm based method for modeling equivalent emission sources of printed circuits from near-field measurements. *2010 Asia-Pacific International Symposium on Electromagnetic Compatibility.*

Yu, Z., Koo, J., Mix, J. A., Slattery, K., & Fan, J. (2010). In Electromagnetic Compatibility (EMC). *IEEE International Symposium*, 317 - 320.

Yu, Z., Mix, J. A., Sajuyigbe, S., Slattery, K. P., & Fan, J. (2013). An improved dipole-moment model based on near-field scanning for characterizing near-field coupling and far-field radiation from an IC. "*Electromagnetic Compatibility, IEEE Transactions on 55*, 97-108.

Zaghloul, H., Papaioannou, G., Coccetti, F., Pons, P., & Plana, R. (2009). Effect of Humidity on Dielectric Charging Process in Electrostatic Capacitive RF MEMS Switches Based on Kelvin Probe Force Microscopy Surface Potential Measurements. *MRS Fall Meeting 2009.* Boston, United States. 6 p., 2009: HAL.

Litvak, B. K. (2011). Noise Versus Coherency in MM-Wave and Microwave Scattering from Inhomogeneous Materials. *Progress in Electromagnetic Research B, Vol. 28*, pp. 35-54.

Pan, J., Li, L., Gao, X., & Fan, J. (2015). Application of dipole-moment model in EMI estimation. *2015 IEEE International Symposium on Electromagnetic Compatibility and EMC Europe* (pp. 350 - 354). Dresden: IEEE.

Poole, I. (2012). Electronic / RF Noise Measurement. *RF Technology and Design*.

Pozar, D. M. (1998). *Microwave Engineering.* John Wiley & Sons.

Society of Cable and Telecomunications Engineers. (2011). *Measurement Procedure for Noise Power Ratio.* Exton, PA: SCTE, Inc.

Timiri, S. (1997). RF Interference Analysis for Collocated Systems. *Microwave Journal*.

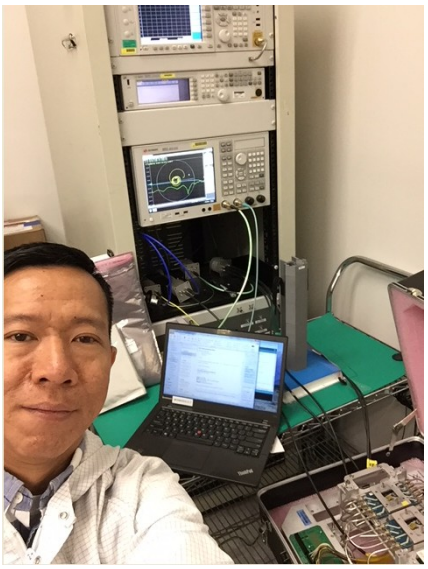
Wilson, P. (1995). On correlating TEM cell and OATS emission measurements. *Electromagnetic Compatibility, IEEE Transactions on 37*, (pp. 1-16).

Xin, T., Nothofer, T. A., Sewell, P., & Christopoulos, C. (2010). A genetic algorithm based method for modeling equivalent emission sources of printed circuits from near-field measurements. *2010 Asia-Pacific International Symposium on Electromagnetic Compatibility.*

Yu, Z., Koo, J., Mix, J. A., Slattery, K., & Fan, J. (2010). In Electromagnetic Compatibility (EMC). *IEEE International Symposium*, 317 - 320.

Annexes

Author's Autobiography



Enrico Marcelo received the B.S. degree in Electronics and Communications Engineering from Technological University of the Philippines – Visayas, Bacolod City, Philippines, in 1996. On the same year, he took the Engineering licensure board exam and able to qualify as a licensed professional electronics and communications engineer.

He worked as an Equipment Engineer in Amkor Technology Philippines and was an equipment designer for Static and Dynamic Life Test Equipment and received a Technical Fellow Award for his several technical works. He also received an Equipment Expert Title following his work on upgrading equipment capabilities to cater customer complex device specification. In the summer of 2003, he worked to establish LSI Space Devices in Guangjong, South Korea. One of his effective researches was on Altera Life Test Process and Design on which the original Life Test boards were rectified. Countless design improvement and analog and digital circuit designs follows for several Amkor customers' platform and all were successfully completed and highly utilized. Had also worked with several scientists, developers and designers to resolve several product issues and was able to contribute to the successes of their product releases. His last task at Amkor Technology Philippines was focused on RF technology where several RF related issues were resolved both on equipment and customer devices. In the year 2011 he started to work as Equipment Engineer Expert level in Skyworks Solutions de Mexico, and was able to complete several projects and designed a process method that contributes at least 4 million USD per year. Upgraded circuitry for several equipment of Front End, Back end and Test were also completed and currently being utilized. His current interest is IC design of Low Phase Noise Oscillators

for RF applications, MEMs IC development and digital VLSI – SOC (system on chip) technologies. All these he brings back to God all the glory, honor and praise.